LISTING OF THE CLAIMS

Claim 1 (Currently Amended): A liquid crystal display device comprising:

a liquid crystal cell which forms an image display area on a substrate; and

a driver for applying a voltage to said liquid crystal cell based on an input video signal, wherein said driver includes a plurality of driver ICs that are mounted on said substrate and a plurality of signal lines, each of the signal lines passing through each of the driver ICs in series, wherein said driver ICs are cascade-connected in series using said signal lines, and wherein the driver receives a digital packet signal including said input video signal and each driver IC includes a controller for generating a mask signal to mask video data output from the driver IC and for transmitting a wait bit block to a succeeding driver IC in said series; and

wherein said plurality of ~~drives~~ driver ICs are cascade-connected to a power feed line via a metal layer inside of each of said driver ICs; and wherein:

during reception of video data, each driver IC transmits the wait bit block to said succeeding driver IC; and

during reception of the wait bit block, said succeeding driver IC does not process any video data and waits to receive video data from said each driver IC.

Claim 2 (Cancelled).

Claim 3 (Original): The liquid crystal display device according to claim 1, wherein said driver ICs receive video signal consisting of serial data, and wherein said video signal is synchronized based on a synchronization pattern included in said serial data.

Claim 4 (Currently Amended): A liquid crystal display device comprising:

a liquid crystal cell which forms an image display area on a substrate; and

a driver for distributing an input video signal to a plurality of driver ICs chain connected in series using a plurality of signal lines, each of the signal lines passing through each of the driver ICs in series, and for applying a voltage to said liquid crystal cell by employing said driver ICs,

wherein said driver receives a digital packet signal including said input video signal and distributes said video signal to said plurality of driver ICs, and each driver IC includes a controller for providing a masking signal to mask the video signal output by said driver IC and for transmitting a wait bit block to a succeeding driver IC in said series; and wherein:

during reception of video data, each driver IC transmits the wait bit block to said succeeding driver IC; and

during reception of the wait bit block, said succeeding driver IC does not process any video data and waits to receive video data from said each driver IC.

Claim 5 (Original): The liquid crystal display device according to claim 4, wherein said downstream driver IC of said driver applies a voltage to said liquid crystal cell in accordance with said input video signal after receiving said masking signal from said upstream driver IC.

Claim 6 (Currently Amended): A liquid crystal display device comprising:

a liquid crystal cell which forms an image display area on a substrate; and

a driver for distributing an input video signal to a plurality of driver ICs that are cascade-connected, and for applying a voltage to said liquid crystal cell by employing said driver ICs,

wherein said plurality of driver ICs of said driver are cascade-connected in series by a video transmission line provided on said substrate, said video transmission line passing through each of the driver ICs in series, and are controlled by serial data that are transmitted along said video transmission line, and wherein the driver receives a digital packet signal including said input video signal and each driver IC includes a controller for generating a mask signal to mask the serial data output from the driver IC and for transmitting a wait bit block to a succeeding driver IC in said series; and

wherein said driver further comprises a clock line and a power line which make a cascade connection to said plurality of driver ICs via a metal layer inside of each of said driver ICs; and wherein:

during reception of video data, each driver IC transmits the wait bit block to said succeeding driver IC; and

during reception of the wait bit block, said succeeding driver IC does not process any video data and waits to receive video data from said each driver IC.

Claim 7 (Original): The liquid crystal display device according to claim 6, wherein said video transmission line connecting said plurality of driver ICs comprises a first signal line, and a second signal line for which the polarity of said first signal line has been inverted.

Claim 8 (Cancelled).

Claim 9 (Original): The liquid crystal display device according to claim 6, wherein, of said driver ICs, an upstream driver IC includes a dummy circuit for substantially matching a video phase and a clock phase.

Claim 10 (Currently Amended): A liquid crystal controller comprising:

a receiver for receiving a video signal from a host to display an image;

a sequencer for, upon the receipt of a control signal from said host, generating header information, based on a table, for packet data that are to be output to an LCD driver comprising a plurality of driver ICs and a video transmission line passing through each of the driver ICs in series, wherein said driver ICs are cascade-connected in series via a metal layer inside of each of said drive ICs; and

output means for converting said video signal received from said receiver into a serial video signal, for adding said header information generated by said sequencer to said serial video signal to form a digital packet signal including said serial video signal, and for outputting the resultant packet signal to the ICs of said LCD driver; and

wherein each driver IC includes a controller for generating a mask signal to mask the serial video signal output from the driver IC and for transmitting a wait bit block to a succeeding driver IC in said series; and wherein:

during reception of video data, each driver IC transmits the wait bit block to said succeeding driver IC; and

during reception of the wait bit block, said succeeding driver IC does not process any video data and waits to receive video data from said each driver IC.

Claim 11 (Previously Presented): A liquid crystal controller comprising:

a receiver for receiving a video signal from a host to display an image;

a sequencer for, upon the receipt of a control signal from said host, generating header information for packet data that are to be output to an LCD driver comprising a plurality of driver ICs and a video transmission line passing through each of the driver ICs in series, wherein said driver ICs are cascade-connected in series; and

output means for converting said video signal received from said receiver into a serial video signal, for adding said header information generated by said sequencer to said serial video signal to form a digital packet signal including said serial video signal, and for outputting the resultant packet signal to the ICs of said LCD driver; and

wherein each driver IC includes a controller for generating a mask signal to mask the serial video signal output from the driver IC; and

wherein said sequencer generates said header information by which said driver ICs of said LCD driver are synchronized with each other, and wherein said output means provide said header information used for synchronization during a horizontal blanking period.

Claim 12 (Currently Amended): A video signal transmission method, for transmitting a video signal to an LCD driver which has a plurality of driver ICs and a video transmission line, comprising the steps of:

transmitting a digital packet signal including a video signal, including a horizontal blanking period, to said driver ICs in series via a serial interface wherein the video transmission line passes through each of the driver ICs in series, and the driver ICs are cascade connected in series by said via a metal layer inside of each of said driver ICs;

transmitting a synchronization pattern during said horizontal blanking period in order to synchronize said video signal for said driver ICs; and

each driver IC selectively generating a mask signal to mask the video signal output from the driver IC and transmitting a wait bit block to a succeeding drier IC in said series; and wherein:

during reception of video data, each driver IC transmitting the wait bit block to said succeeding driver IC; and

during reception of the wait bit block, said succeeding driver IC not process any video data and waits to receive video data from said each driver IC..

Claim 13 (Previously Presented): A video signal transmission method, for transmitting a video signal to an LCD driver which has a plurality of driver ICs and a video transmission line, comprising the steps of:

transmitting a digital packet signal including a video signal, including a horizontal blanking period, to said driver ICs in series via a serial interface wherein the video transmission line passes through each of the driver ICs in series, and the driver ICs are cascade connected in series by said video transmission line;

transmitting a synchronization pattern during said horizontal blanking period in order to synchronize said video signal for said driver ICs; and

each driver IC selectively generating a mask signal to mask the video signal output from the driver IC; and

wherein said synchronization pattern is transmitted for at least at two cycles, and wherein, during the period in which said video signal is transmitted, said driver ICs conform to said synchronization pattern.

Claim 14 (Cancelled).

Claim 15 (Previously Presented): A video signal transmission method, for transmitting a video signal to an LCD driver which has a plurality of driver ICs that are cascade-connected, comprising the steps of:

transmitting a digital packet signal including a video signal via a serial interface to said driver ICs that are cascade-connected in series by a video transmission line passing through each of the driver ICs in series;

applying to an LCD a voltage based on said video signal that is received and that is to be processed by each of said driver ICs; and

each driver IC selectively generating a mask signal to mask the video signal output from the driver IC; and

wherein said video signal is constituted by bit blocks having a plurality of attributes and wherein said driver ICs are controlled by using said bit blocks; and

wherein one of said bit blocks includes a wait command for waiting for said driver ICs, and wherein said wait command is generated by each of said driver ICs that processes said video signal, and is transmitted to a downstream driver IC that is cascade-connected.

Claim 16 (Currently Amended): ~~The~~ A video signal transmission method ~~according to claim 14,~~ for transmitting a video signal to an LCD driver which has a plurality of driver Ics that are cascade-connected via a metal layer inside of each of said driver ICs, comprising the steps of:

transmitting a digital packet signal including a video signal via a serial interface to said driver ICs that are cascade-connected in series by a video transmission line passing through each of the driver ICs in series;

applying to an LCD a voltage based on said video signal that is received and that is to be processed by each of said driver ICs;

each driver IC selectively generating a mask signal to mask the video signal output from the driver IC and transmitting a wait bit block to a succeeding driver IC in said series;

wherein said video signal is constituted by bit blocks having a plurality of attributes and wherein said driver ICs are controlled by using said bit blocks; and

wherein said video signal is transmitted to said LCD driver by using a packet, and wherein said plurality of driver ICs are controlled by a protocol that employs the header of said packet.

Claim 17 (Cancelled).